MM74HC157 Quad 2-Input Multiplexei

MM74HC157 Quad 2-Input Multiplexer

General Description

FAIRCHILD

SEMICONDUCTOR

The MM74HC157 high speed Quad 2-to-1 Line data selector/Multiplexers utilizes advanced silicon-gate CMOS technology. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

This device consists of four 2-input digital multiplexers with common select and STROBE inputs. When the STROBE input is at logical "0" the four outputs assume the values as selected from the inputs. When the STROBE input is at a logical "1" the outputs assume logical "0".

The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to $\rm V_{CC}$ and ground.

Features

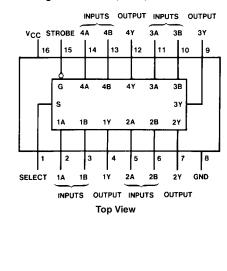
- Typical propagation delay: 14 ns data to any output
- Wide power supply range: 2–6V
- Low power supply quiescent current: 80 µA maximum (74HC Series)
- Fan-out of 10 LS-TTL loads
- Low input current: 1 µA maximum

Ordering Code:

Order Number	Package Number	Package Description		
MM74HC157M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow		
MM74HC157SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide		
MM74HC157MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide		
MM74HC157N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide		
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.				

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Function Table

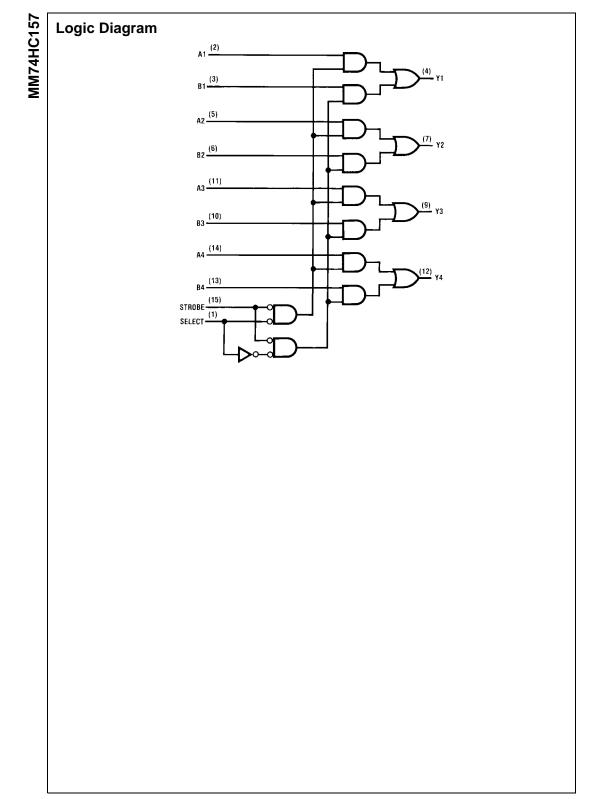
Inputs				Output
Strobe	Select	Α	В	Y
Н	Х	Х	Х	L
L	L	L	Х	L
L	L	н	Х	н
L	н	Х	L	L
L	н	Х	н	н



X = Irrelevant

© 1999 Fairchild Semiconductor Corporation DS005314.prf

www.fairchildsemi.com



Absolute Maximum Ratings(Note 1)

Recommended Operating Conditions

	0
(Note 2)	
Supply Voltage (V _{CC})	-0.5 to +7.0V
DC Input Voltage (V _{IN})	-1.5 to $V_{CC}{+}1.5V$
DC Output Voltage (V _{OUT})	–0.5 to V_{CC} +0.5V
Clamp Diode Current (I _{IK} , I _{OK})	±20 mA
DC Output Current, per pin (I _{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I _{CC})	±50 mA
Storage Temperature Range (T _{STG})	$-65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation (P _D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (TL)	
(Soldering 10 seconds)	260°C

	Min	Max	Units			
Supply Voltage (V _{CC})	2	6	V			
DC Input or Output Voltage	0	V_{CC}	V			
(V _{IN} , V _{OUT})						
Operating Temperature Range (T_A)	-40	+85	°C			
Input Rise or Fall Times						
$(t_r, t_f) V_{CC} = 2.0V$		1000	ns			
$V_{CC} = 4.5V$		500	ns			
$V_{CC} = 6.0V$		400	ns			
Note 1: Absolute Maximum Ratings are those values beyond which dam-						

MM74HC157

age to the device may occur. Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: – 12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	v _{cc}	$T_A = 25^{\circ}C$		$T_A = -40$ to 85°C $T_A = -55$ to 125		C Units
Symbol				Тур	Guaranteed Limits		imits	
VIH	Minimum HIGH Level		2.0V		1.5	1.5	1.5	V
	Input Voltage		4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
VIL	Maximum LOW Level		2.0V		0.5	0.5	0.5	V
	Input Voltage		4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V _{OH}	Minimum HIGH Level	$V_{IN} = V_{IH} \text{ or } V_{IL}$						
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$						
		I _{OUT} ≤ 4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		I _{OUT} ≤ 5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V _{OL}	Maximum LOW Level	$V_{IN} = V_{IH} \text{ or } V_{IL}$						
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$						
		I _{OUT} ≤ 4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
	Current							
I _{CC}	Maximum Quiescent	$V_{IN} = V_{CC}$ or GND	6.0V		8.0	80	160	μΑ
	Supply Current	$I_{OUT} = 0 \ \mu A$						

Note 4: For a power supply of 5V \pm 10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

www.fairchildsemi.com

AC Electrical Characteristics

V_{CC}=5V, T_A=25°C, C_L=15 pF, $t_r = t_f = 6 \text{ ns}$ Symbol Parameter

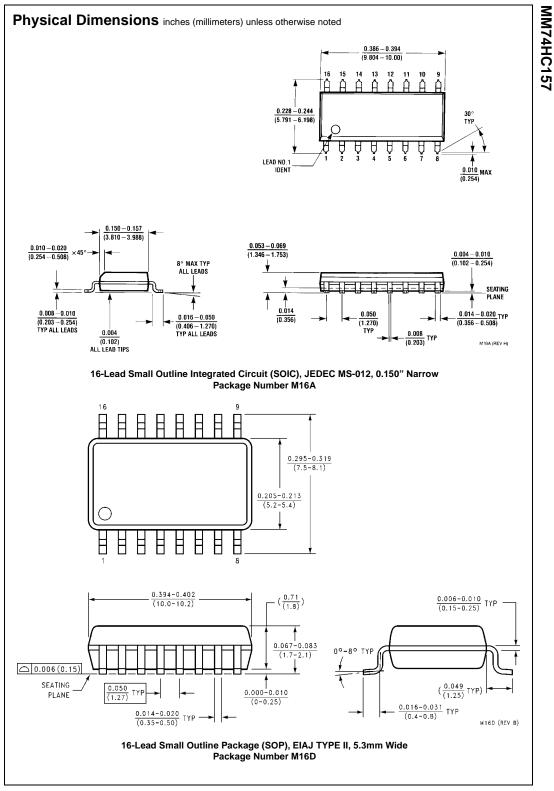
Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
t _{PHL} , t _{PLH}	Maximum Propagation		14	20	ns
	Delay, Data to Output				
t _{PHL} , t _{PLH}	Maximum Propagation		14	20	ns
	Delay, Select to Output				
t _{PHL} , t _{PLH}	Maximum Propagation		12	18	ns
	Delay, Strobe to Output				

AC Electrical Characteristics

 $C_L = 50 \text{ pF}, t_r = t_f = 6 \text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	v _{cc}	$T_A = 25^{\circ}C$		$T_A = -40$ to $85^{\circ}C$	$T_A = -55$ to $125^{\circ}C$	Units	
				Typ Guaranteed Limits			imits	01113	
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	63	125	158	186	ns	
	Delay, Data to Output		4.5V	13	25	32	37	ns	
			6.0V	11	21	27	32	ns	
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	63	125	158	186	ns	
	Delay, Select to Output		4.5V	13	25	32	37	ns	
			6.0V	11	21	27	32	ns	
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	58	115	145	171	ns	
	Delay, Strobe to Output		4.5V	12	23	29	34	ns	
			6.0V	10	20	25	29	ns	
t _{TLH} , t _{THL}	Maximum Output Rise		2.0V	30	75	95	110	ns	
	and Fall Time		4.5V	8	15	19	22	ns	
			6.0V	7	13	16	19	ns	
C _{IN}	Maximum Input			5	10	10	10	pF	
	Capacitance								
C _{PD}	Power Dissipation	(per		57				pF	
	Capacitance (Note 5)	Multiplexer)							

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.



www.fairchildsemi.com

